鋰電池保護IC Delay Time 定義說明

Reported
FAE Dept.

Date
Dec. 12th 2022

常見狀況

AENEAS

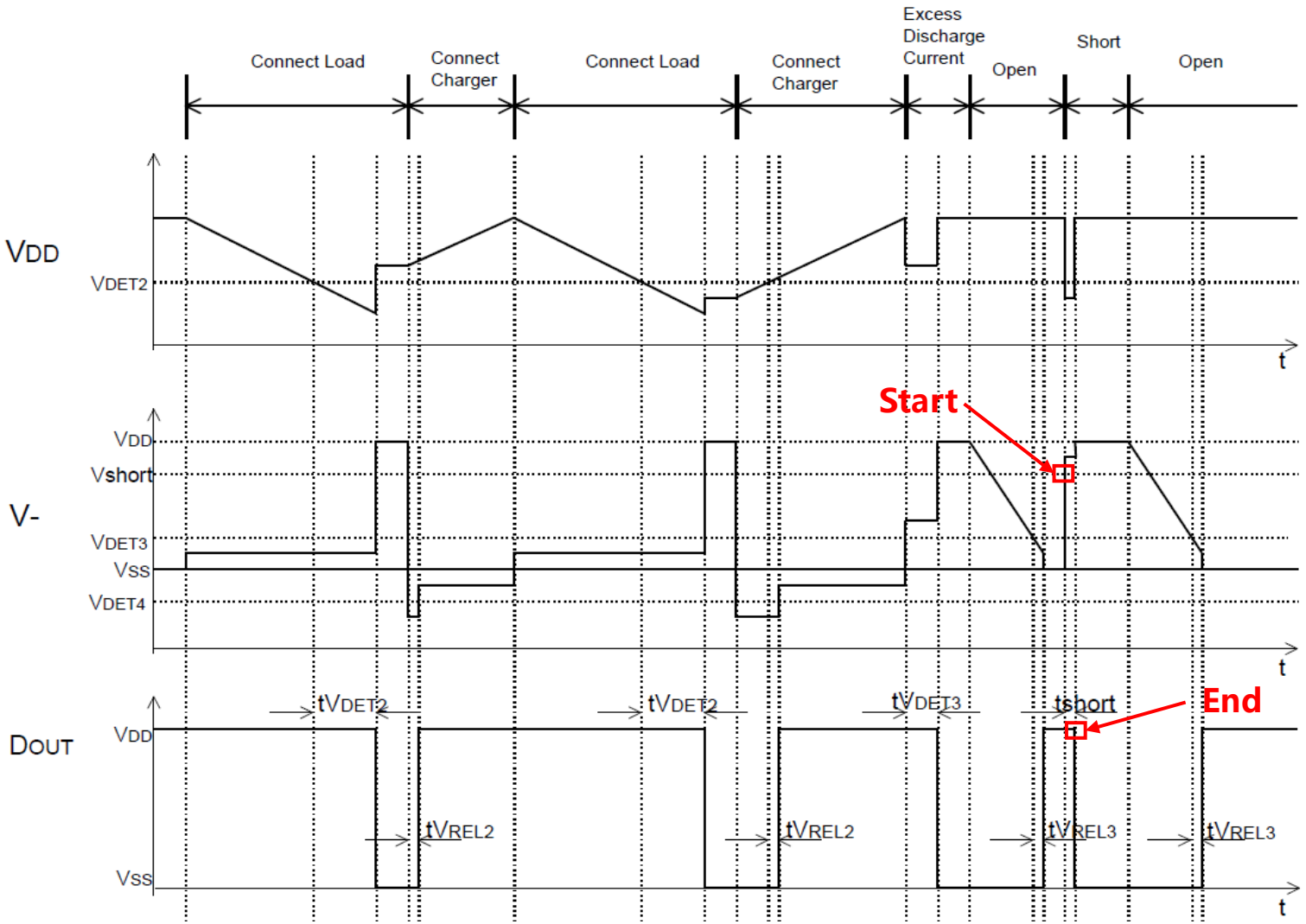
Customer:
What is the root cause of delay time over maximum spec during SCP test?

Ans:
According to this waveform, we can only see that battery pack (P+) was turned off by DFET after short circuit, but cannot understand the real tshort time.
The definition of tshort is start from V- rise to Vshort (0.185V) until DOUT start falling to logic low.
Please see the timing chart in page 3.

Short Protection Voltage	Vshort	Detect rising edge of 'V-' pin voltage	0.180	0.185	0.190	V	F
Delay Time for Short Protection	tshort	V_{DD}=3.0V, V-=0V to 0.50V	210	280	350	µs	F

tshort定義

(2) Over-discharge, Excess discharge current, Short circuit

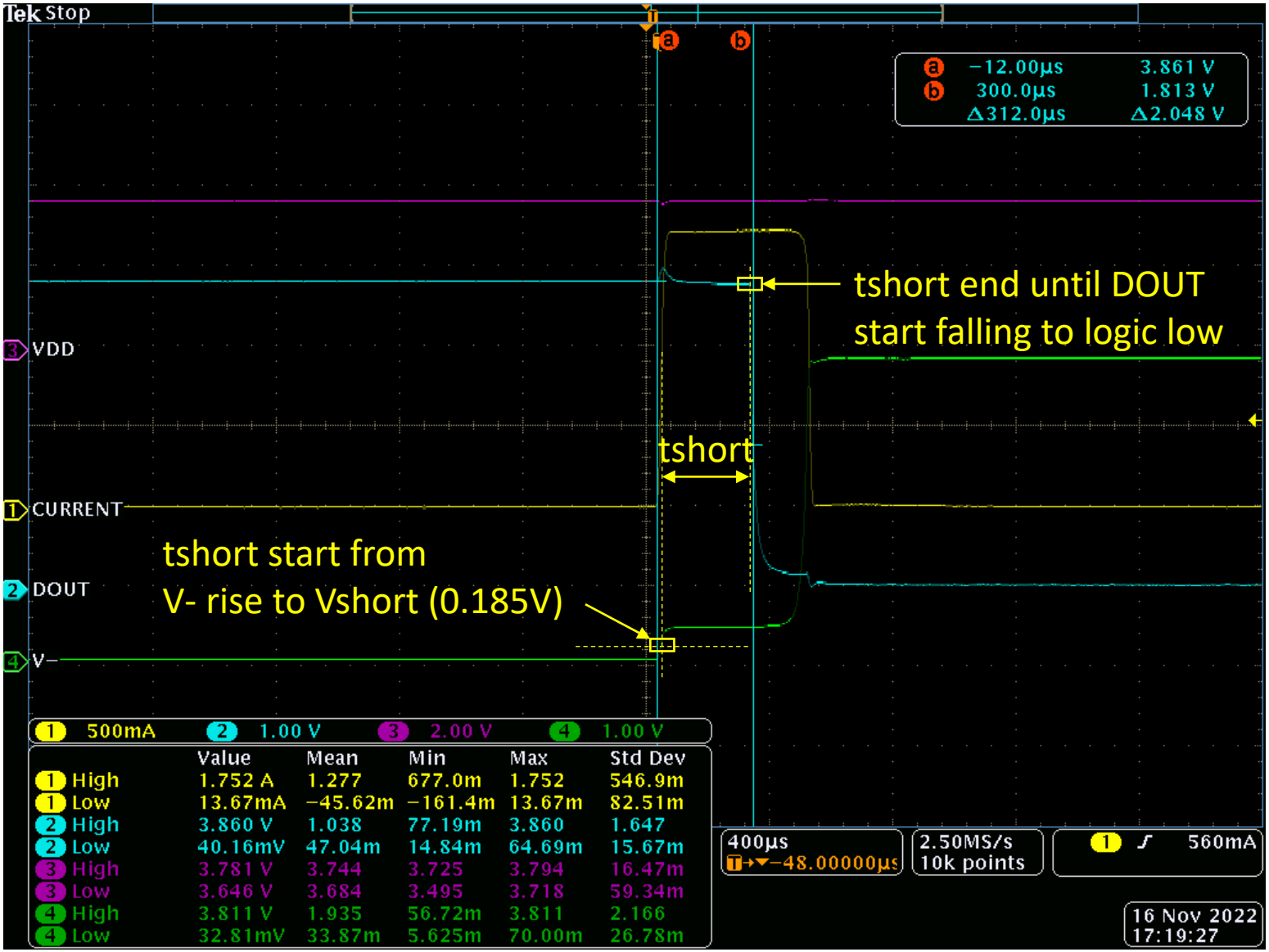


Customer:
What is reason that SCP protection time is 576us, but not within 350us?

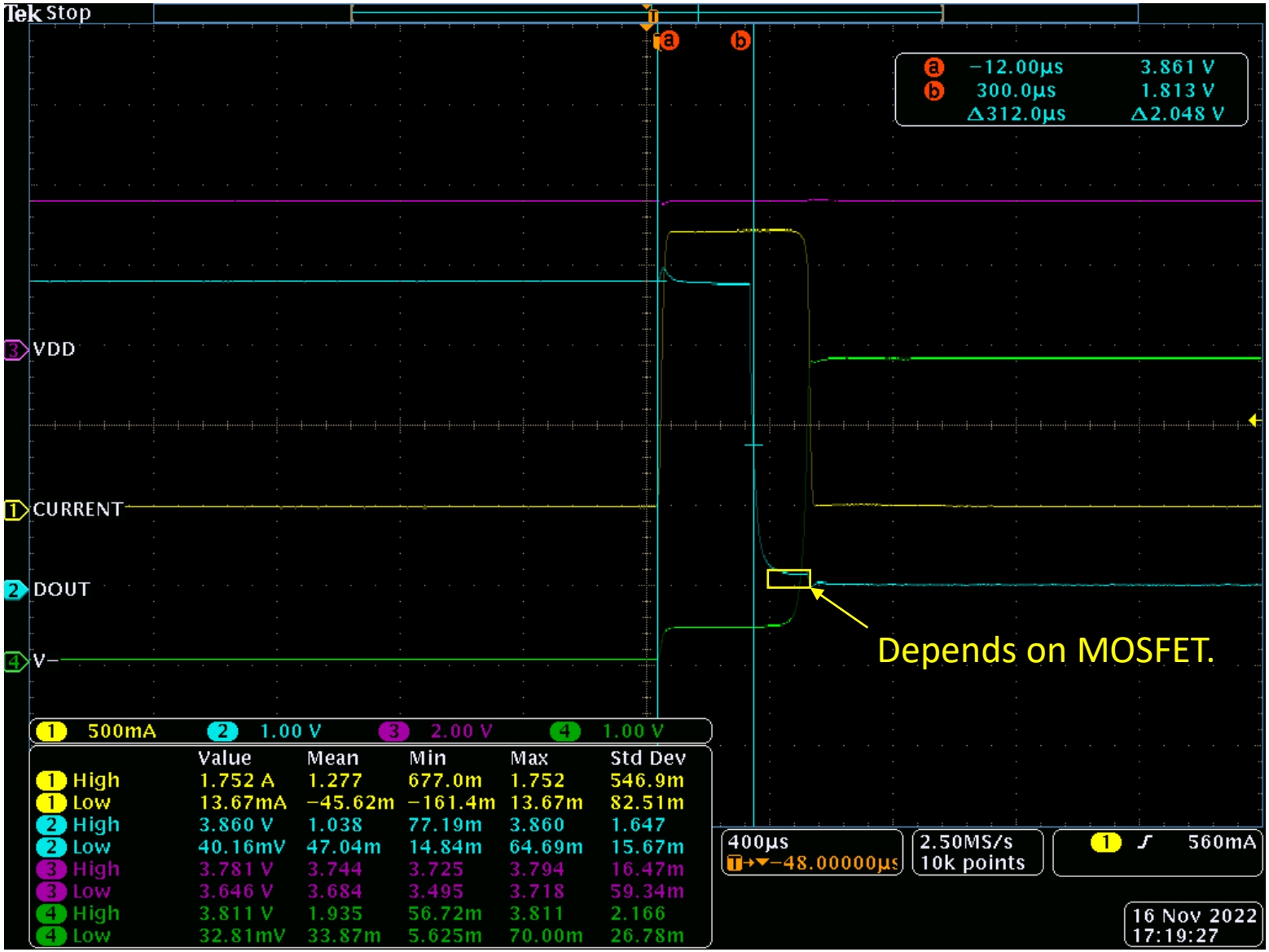
Ans:
tshort is the definition of IC behavior, your waveform is battery pack (system) level measurement.
The time scale is microsecond level, delay time is easily longer than IC measurement level.
Also, a part of delay relates to MOSFET.
According to the correct measurement, tshort is within the spec.
Please see the detail in page 5 and page 6.

For total battery pack point of view, it is better to evaluate the SCP delay time with whole circuit.

tshort定義說明 - 1



tshort定義説明 - 2



Thank You!